## In the Claims:

Please cancel claims 3 and 15-20 without prejudice or disclaimer:

Please amend claims 1-2, 6-8 and 9-12 as follows:

Claim 1 (currently amended) A method for manufacturing multi-level interconnection lines of <u>a</u> semiconductor device comprising:

forming a first interconnection line in a second interlayer insulating layer and a first etching stop layer sequentially formed on a first interlayer insulating layer of disposed on a semiconductor substrate;

forming a first third interlayer insulating layer on the first interconnection line and the second interlayer insulating layer;

forming a first second etching stop layer on the first third interlayer insulating layer;

forming a via hole exposing the first interconnection line by selectively etching the first second etching stop layer and the first third interlayer insulating layer;

forming <u>an</u> etching stop <u>patterns</u> pattern around an inlet of the via hole by selectively etching the <u>first second</u> etching stop layer;

forming a second <u>fourth</u> interlayer insulating layer on the etching stop <del>pattern</del> patterns and the <del>first</del> third interlayer insulating layer;

forming a trench by selectively etching the second fourth interlayer insulating layer; and

forming a conductive layer in the trench and in the via hole.

Claim 2 (currently amended) The method of claim 1, wherein the method further comprises:

forming a photoresist pattern around the inlet of the via hole to cover portions of the first second etching stop layer; and

removing other portions of the first second etching stop layer which are not covered with the photoresist pattern, whereby the etching stop patterns are formed.

Claim 3 (currently canceled)

Claim 4 (original) The method of claim 1, wherein the trench exposes portions of the etching stop patterns at the bottom thereof.

Claim 5 (original) The method of claim 1, wherein the width of the trench is wider than that of the via hole.

Claim 6 (currently amended) The method of claim 1, wherein a void is formed within the via hole in <u>during</u> the step of forming the second <u>fourth</u> interlayer insulating layer.

Claim 7 (currently amended) The method of claim 6, wherein the second fourth interlayer insulating layer is formed with any one selected from the group consisting of an USG layer deposited by the <u>a</u> high density plasma, an oxide deposited by plasma enhance enhanced chemical vapor deposition method or low pressure chemical vapor deposition.

Claim 8 (currently amended) The method of claim 6, wherein the second fourth interlayer insulating layer is formed at a thickness ranging from about 3000 Å to about 30000 Å.

Claim 9 (currently amended) The method of claim 1, wherein the first to third interlayer insulating layer is layers are formed with any one selected from the group consisting of a spin on glass layer, an oxide layer deposited by a plasma enhance enhanced chemical vapor deposition method, an oxide layer deposited by a high density plasma method and a tetra-ethyl-ortho-silicate(TEOS) layer.

Claim 10 (currently amended) The method of claim 9, wherein the first to third interlayer insulating layer is layers are formed at a thickness ranging from about 2000 3000 Å to about 30000 Å.

Claim 11 (currently amended) The method of claim 1, wherein the first second etching stop layer is formed with any one selected from the group consisted of a nitride layer deposited by a plasma enhance enhanced chemical vapor deposition method, a SiON layer, a Ta<sub>2</sub>O<sub>5</sub> layer, a ZnO<sub>2</sub> layer, a ZrO<sub>2</sub> layer, a ZnO layer, a HfO layer and an Al<sub>2</sub>O<sub>3</sub> layer.

Claim 12 (currently amended) The method of claim 11, wherein the first second etching stop layer is formed at a thickness ranging from about 200 Å to about 3000 Å.

Claim 13 (original) The method of claim 1, wherein the first interconnection line is formed of any one selected form a group consisting of Al, Cu, Au, Ag and Cr.

Claim 14 (original) The method of claim 1, the first interconnection line is formed at a thickness ranging from about 2000 Å to about 30000 Å.

Claims 15-20 (currently canceled)